REMARKS

The above amendment amends the specification to correct errors and improve clarity. No new matter is added.

Claims 1-19 were pending in the above-identified application when last examined and are amended as indicated above. The claim amendments clarify the claim language and are not intended to limit the scope of the claims.

Claims 7-9, 15, and 17 were objected to for containing informalities and are amended to add ending periods as the Examiner required. Accordingly, reconsideration and withdrawal of the objection to the claims is requested.

Claims 1-19 were rejected under 35 U.S.C. § 112, second paragraph. In particular, the Examiner indicated that the phrase "wherein the current blocking region operates as a reverse bias PN junction" in claim 1 and the phrase "the current blocking region acts as a reverse biased PN junction" in claim 11 did not provide clear limitations of recited structure or step. To improve clarity, claim 1 is amended to recite, "wherein the current blocking region comprises a PN junction that is reverse biased during operation of the optoelectronic device." Claim 11 is amended to recite, "wherein the current blocking region comprises a PN junction that is reverse biased during operation of the optoelectronic device and restricts current between the active region and the semiconductor region." Claim 2-10 and claims 12-19, which were rejected for depending from claims 1 and 11, comply with the requirements of 35 U.S.C. § 112, second paragraph.

In view of these amendments, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 112.

Claims 1, 10, 11, and 19 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,046,065 (Goldstein et al.) Applicants respectfully traverse the rejection.

Independent claim 1 distinguishes over Goldstein et al. at least by reciting, "a current blocking region ... comprises a PN junction that is reverse biased during operation of the optoelectronic device and confines a current between the active region and the semiconductor region to the current through the tunnel junction." Goldstein et al. fails to disclose a current blocking region comprising a PN junction that is reverse bias.

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Figs. 1 and 2 of Goldstein et al. illustrate optoelectronic devices. Both devices include areas 8 that control current. In particular, Goldstein et al. starting at column 6, line 33 states, "The peripheral area of this layer is oxidized to constitute a dielectric screen 8 of AlOx used to confine or to uniformize the excitation current density." Goldstein et al. thus describes using an oxide or insulator to control current. However, Goldstein fails to disclose or suggest "the current blocking region comprises a PN junction that is reverse biased" as recited in claim 1. Accordingly, claim 1 and claim 10, which depends from claim 1, are patentable over Goldsteing et al.

Independent claim 11 distinguishes over Goldstein et al. at least by reciting, "disabling tunneling in a selected part of the tunnel junction to form a current blocking region." In regard to a tunneling junction, Goldstein et al. starting at column 7, line 10 states, "In the fourth laser, ... The layers 7, 9 and 11 are also n-doped and the excitation current is transmitted via an n/p tunnel junction formed by the layers 5 and 7." Goldstein et al. fails to teach or suggest disabling part of the tunnel junction. As noted above, Goldstein et al. uses a separate oxide region 8 to confine current. Accordingly, claim 11 and claim 19, which depends from claim 11, are patentable over Goldstein et al.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102.

Claims 1-19 were rejected under 35 U.S.C. § 102(b) as anticipated by Published PCT International Publication No. WO 98/07218 (Gore). Applicants respectfully traverse the rejection.

Gore is directed to VCSELs that contain tunneling junctions, and Gore discloses using either insulating or resistive regions to control the current distribution in the VCSELs. For example, Fig. 2 of Gore illustrates a VCSEL that "is implant-constricted for current confinement." (See page 5, lines 18-19 of Gore.) "A tunnel junction interface 48 is formed above p-doped GaAs layer 46." (See page 6, lines 10-11.) "Protons (H+) are implanted along an annular section 56 of top n-type mirror stack 38 at tunnel junction interface 48. ... Annular section 56 has a higher electrical resistivity than other parts of top n-type mirror stack 38 and constricts current flow to within the annular section." (See page 6, lines 20-25.) In the alternative embodiments illustrated in Figs. 3 and 4, Gore discloses using an oxidation layer 90 or 114. See Gore starting at page 8, line 14 and starting at page 9, line 21.

Independent claim 1 distinguishes over Gore at least by reciting, "a current blocking region between the active region and the semiconductor region, wherein the

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current blocking region comprises a PN junction that is reverse biased during operation of the optoelectronic device and confines a current between the active region and the semiconductor region to the current through the tunnel junction." As noted above, Gore discloses use of resistive or insulating regions for current confinement, but Gore fails to disclose a current blocking region comprising a PN junction that is reverse bias.

The Gore patent refers to an ion implant, where the stated intent is to increase the resistivity in that region. In the standard practice, such ion implants increase the bulk material resistivity of the semiconductor layer and are close to the tunnel junction for the purpose of confining current more precisely, e.g., limiting current spreading between the implanted layer and the tunnel junction layer. Gore fails to discuss or suggest disruption of the tunneling action as the result of the ion implant and fails to suggest forming a reverse biased PN junction.

As noted in Applicants' specification, current constriction can be achieved through reduction of the tunneling action by disruption of the tunnel junction interface, creating a reverse biased PN junction. This modification of the tunnel junction does not require significant bulk resistivity change and therefore may provide effective confinement with lower implant dose, possibly resulting in more reliable VCSELs. Gore fails to disclose or suggest the use of reverse bias PN junctions for current confinement or the attendant advantages. Accordingly, claim 1 is patentable over Gore.

Claims 2-10 depend from claim 1 and are patentable over Gore for at least the same reasons that claim 1 is patentable over Gore. Claim 9 further distinguishes over Gore by reciting, "the current blocking region comprises a portion of the tunnel junction that has been partially diffused by impurity-free disordering." Gore fails to provide any suggestion of impurity-free disordering.

Independent claim 11 distinguishes over Gore at least by reciting, "disabling tunneling in a selected part of the tunnel junction to form a current blocking region, wherein the current blocking region comprises a PN junction that during operation of the optoelectronic device, is reverse biased and restricts current between the active region and the semiconductor region." As noted above, Gore fails to disclose or suggest a current blocking region comprising a PN junction that is reverse biased. Accordingly, claim 11 and claims 12-19, which depend from claim 11, are patentable over Gore.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102.

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In summary, claims 1-19 were pending in the application. This response amends claims 1, 7-9, 11, 15, and 17 to improve clarity. For the above reasons, Applicants respectfully request allowance of the application including claims 1-19.

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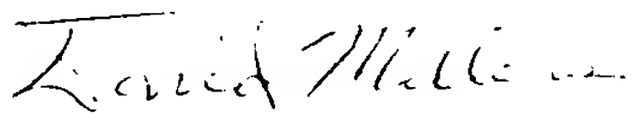

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